AMENDMENTS TO THE DRAWINGS

The attached sheet of drawings includes changes to FIG. 13. This sheet, which includes FIG. 13, replaces the original sheet including FIG. 13. In FIG 13, the reference number 152 has been deleted.

Attachment: Replacement Sheet
Annotated Sheet Showing Changes

REMARKS

Applicant respectfully requests reconsideration and allowance of the subject application. Claims 1-6 and 14-18 are cancelled. Claim 19 is amended. Claims 22-33 are added. Claims 7-13 and 19-33 are pending.

Objections

The Office objected to the title of the invention as not descriptive. The Applicant has amended the title. Therefore, withdrawal of the objection is respectfully requested.

The Office objected to the specification. The Applicant has amended the specification. Therefore, withdrawal of the objection is respectfully requested.

The Office objected to the drawings, and in particular FIG. 13. A replacement FIG. 13 is included along with an annotated version showing changes made to FIG. 13 to remove reference number "152" as requested by the Office. Therefore, withdrawal of the objection is respectfully requested.

The Office objected to claims 3 and 6. The Applicant has cancelled claims 3 and 6, thereby obviating the objection.

35 U.S.C. §102

Claims 1-6 are rejected under 35 U.S.C. §102 as being anticipated by Liu et. al, (U.S. 2003/0081070), hereinafter, "Liu"). The Applicant has cancelled claims 1-6, thereby obviating the rejection.

35 U.S.C. §102

Claims 7, 9-13 are rejected under 35 U.S.C. §102 as being anticipated by U.S. Patent No. 6,200,862 to Gardner et al. (hereinafter, "Gardiner"). Applicant respectfully traverses the rejection.

Claim 7 is directed to "depositing a layer of oxide proximate a first surface of a semiconductor substrate", "forming a gate oxide layer on the first surface, adjacent to the deposited oxide layer", "forming a pair of active areas in the first surface, adjacent the deposited oxide layer and gate oxide layer", "forming a gate electrode by depositing a conductive layer over the gate oxide layer", "depositing a dielectric layer over the gate electrode, active areas, and deposited oxide layer", and "forming electrical contacts to the pair of active areas and the gate electrode". Gardner does not disclose these aspects.

Gardiner is directed to a mask for asymmetrical transistor formation with paired transistors. Gardiner discloses the first step for producing the transistor as follows:

> Substrate 10 has already had formed therein, e.g., by ion implantation, a channel region 14, a punch-through region, and a well region. (Only the channel region 14 is illustrated.) The substrate can be doped with arsenic or phosphorous ions to form an n-doped channel regions (or n-channel regions). The substrate can be doped with boron ions to form a p-doped channel (or p-channel) regions. *Gardiner, Col. 3, Lines 24-31.*

Gardiner then discloses that "[a]fter formation of doped regions in the substrate 10, a gate dielectric layer 22, of 10-30 ANG. is formed by oxide growth, plasma deposition, or low pressure chemical vapor deposition." *Gardiner, Col 3, Lines 52-55.* Gardiner then discloses a patterning of layer 30 for ion bombardment to form a resulting device having asymmetric source/drain regions. *See Gardiner,*

Col. 4, Lines 14-36. Gardiner then discloses formation of a dielectric layer as follows:

> The photoresist regions 30 are removed and a dielectric layer 40, typically silicon oxide is formed and planarized. Vias are formed in the dielectric layer 40 exposing the surfaces of the substrate source/drain regions 28[1], 34 and the surfaces of the gate electrode of gate structure 20. *Gardiner, Col 4, Lines 40-44.*

Thus, Gardiner discloses the formation of the dielectric layer 40, but is silent to the aspect of "depositing a layer of oxide proximate a first surface of a semiconductor substrate" as claimed in Claim 7.

Nowhere in Gardiner is there discussion, teaching or suggestion for deposition of the oxide as claimed in claim 7. The Office asserted column 4, lines 24-31 of Gardiner for support of depositing a layer of oxide 40 proximate a first surface of a semiconductor substrate. As shown in the portion excepted above, Gardiner refers to a "[s]ubstrate 10 that has already had formed therein, e.g., by ion implantation, a channel region 13, a punch-through region, and a well region." *Gardiner, Col. 3, Lines 24-27.* This is simply a general statement regarding the substrate, and does not disclose, teach or suggestion deposition of the oxide as claimed in claim 7.

For these reasons, claim 7 is allowable over Gardiner. Applicant respectfully requests that the §102 rejection of claim 7 be withdrawn.

Claims 8-13 depend from claim 7 and are allowable by virtue of this dependency.

35 U.S.C. §102

Claims 19-21 are rejected under 35 U.S.C. §102 as being anticipated by U.S. Patent No. 6,485,132 to Hiroki et al. (hereinafter, "Hiroki"). Applicant respectfully traverses the rejection.

Claim 19, as amended, is directed to "depositing a current prevention layer proximate a first surface of a semiconductor substrate" and "forming first and second field effect transistors (FETs) on the substrate having the current prevention layer, wherein each said FET includes a gate electrode with associated active areas formed in the first surface of the semiconductor substrate, wherein the current prevention layer includes a region that minimizes current flow between the active areas of the first FET with respect to the active areas of the second FET." Hiroki does not disclose these aspects.

Hiroki is directed to a liquid discharge head, recording apparatus and method for manufacturing liquid discharge heads. The Office asserts "current prevention layer 416 (i.e. a silicon oxide layer) on the first surface in between the first (i.e. 406 of 450) and second (i.e. 405 of 451) active areas." The interlayer insulation layer 416 of Hiroki, however, is installed "[a]fter each of the elements is formed". *Hiroki, Col. 9, Line 20.* Claim 19 as amended recites "forming first and second field effect transistors (FETs) *on the substrate having the current prevention layer*" (emphasis added). Claim 19 as amended then recites that "first and second field effect transistors (FETs) ... [are] formed in the first surface of the semiconductor substrate having the deposited current prevention layer".

For these reasons, claim 19 is allowable over Hiroki. Applicant respectfully requests that the §102 rejection of claim 19 be withdrawn.

Claims 20-21 depend from claim 19 and are allowable by virtue of this dependency.

35 U.S.C. §103

Claims 14-18 are rejected under 35 U.S.C. §103 as being unpatentable over Liu in view Hiroki. Applicant has cancelled claims 14-18, thereby obviating the rejection.

New Claims

The Applicant has submitted new claims 22-33. Each of the newly added claims is supported by the specification and drawings as filed.

Claim 22 is an independent claim that recites "depositing a layer of oxide proximate a first surface of a semiconductor substrate", "exposing a portion of the first surface of the semiconductor substrate", and "forming a field effect transistor (FET) on the exposed portion of the first surface of the substrate having the deposited oxide layer, wherein the FET includes a gate electrode with associated active areas formed in the first surface of the semiconductor substrate". Claim 22 is supported throughout the specification and drawings as filed, such as in FIGS. 1-6a and the accompanying discussion. None of the submitted references, either alone or in combination, teach depositing, exposing and forming as claimed. Therefore, claim 22 is allowable over the submitted references.

Claim 23 depends from claim 22 and is allowable by virtue of this dependency.

Claim 24 is an independent claim that recites "depositing a layer of oxide proximate a first surface of a semiconductor substrate", "exposing a portion of the

first surface of the semiconductor substrate", "forming a gate oxide layer on the exposed portion of the first surface, adjacent to the deposited oxide layer", "forming a pair of active areas in the exposed portion of the first surface, adjacent the deposited oxide layer and gate oxide layer", "forming a gate electrode by depositing a conductive layer over the gate oxide layer", "depositing a dielectric layer over the gate electrode, active areas, and deposited oxide layer", and "forming electrical contacts to the pair of active areas and the gate electrode." Claim 24 is supported throughout the specification and drawings as filed, such as in FIGS. 1-6a and the accompanying discussion. None of the submitted references, either alone or in combination, teach depositing and exposing as claimed. Therefore, claim 24 is allowable over the submitted references.

Claims 25–31 depend from claim 24 and are allowable by virtue of this dependency.

Claims 32 and 33 depend from independent claims 7 and 19 respectively, and are allowable by virtue of the respective dependencies.

Conclusion

All pending claims 7-13 and 19-33 are in condition for allowance. Applicant respectfully requests reconsideration and prompt issuance of the subject application. If any issues remain that prevent issuance of this application, the Examiner is urged to contact the undersigned attorney before issuing a subsequent Action.

Respectfully submitted,

Dated: 7/31/2003

By: _____

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Attachment: Replacement Sheet of FIG. 13.
Annotated Sheet Showing Changes